REMARKS/ARGUMENTS

Claim Status and Amendment to the Claims

Claims 1-3, 8-10, 15-17 and 22-50 are now pending. No claims stand allowed.

Claims 4-7, 11-14 and 18-21 have been cancelled by this amendment, without prejudice.

Claims 1-3, 8-10, 15-17 and 22-25 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. The text of claim 26 is unchanged, but its meaning is changed because they depend from amended claims.

New claims 27-50 have been added by this amendment and also particularly point out and distinctly claim subject matter regarded as the invention.

The amendment also contains minor changes of a clerical nature.

The amendments to the claims and new claims are supported by the description in paragraphs [0035] through [0052] and FIGS. 5-10B, for example. No "new matter" has been added by the amendment.

Amendment to the Specification

In the specification, paragraph [0048] has been amended to clarify the function of the XOR in the transmitting BSC 502. The function of the elements in the BSC 502 is well understood by one of ordinary skill in the art from FIG. 5 and the related description of the specification. The correction does not add "new matter".

Objection to the Drawings

The drawings stand objected to for FIGS. 1 and 2 should be designated by a

legend such as --Prior Art--. FIGS. 1 and 2 have been amended to be labeled as "PRIOR ART" in accordance with the Examiner's suggestion. With this amendment, withdrawal of the objection is respectfully requested.

Objections to the Claims

Claims 5, 12 and 19 stand objected to because of certain informalities. The objected claims have been cancelled without prejudice. Withdrawal of the objection to the claims is respectfully requested.

The 35 U.S.C. §103 Rejection

Claims 1-26 stand rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Wu et al. (U.S. Pat. No. 6,286,119) in view of Miller (U.S. Pat. No. 6,606,575), among which claims 1, 8, 15 and 22-25 are independent claims.

This rejection is respectfully traversed.

According to M.P.E.P. §2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

1. Regarding Claims 1, 8 and 15

Claim 1, as amended, defines a method for testing a circuit including AC coupled interconnects, the circuit having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having a Boundary Scan Cell (BSC) connected to a reference clock. The claimed method comprises (a) generating an AC signal based on the reference clock and a value held in the BSC of the transmitting IC, the AC signal having a first phase if a first value is held in the BSC holds, and a second phase if a second value is held in the BSC, (b) generating, for the receiving IC, a sync pulse signal based on a test reset signal, (c) capturing, in the BSC of the receiving IC, a default phase of said AC signal in response to said sync pulse signal, (d) sampling a phase of the AC signal, (e) comparing the default phase with the sampled phase of the AC signal, and (f) generating a phase decode signal based on said comparing, as recited in claim 1 as amended.

Wu allegedly teaches interconnect delay fault tests for IC chips (Abstract, column 4, line 63 thereof). Although Wu captures signals at the rising edge of the scan test clock control signal and stores them in BSCs (column 2, lines 58-64, column 5, lines 25-34 thereof), Wu does not teach or suggest any signal having a first phase or a second phase depending on a value held in the BSC. As shown in FIGS. 3 and 13 thereof, some signals in Wu may be delayed, but no AC signal in Wu changes its phase. Thus, Wu fails to teach or suggest generating an AC signal based on the reference clock and a value held in the BSC of the transmitting IC, where the AC signal has a first phase if a first value is

held in the BSC holds, and a second phase if a second value is held in the BSC, as recited in claim 1.

In addition, as the Examiner correctly noted in the Office Action, Wu also fails to teach or suggest comparing the default phase with the sampled phase of the AC signal, and generating a phase decode signal based on said comparing, as recited in claim 1.

Miller allegedly teaches comparing a test signal pattern with a reference signal pattern which has the same edge pattern as the test signal (Abstract thereof). In Miller, the test signal and the reference signal are correlated, and a MACH signal is produced (column 8, lines 2-19, FIGS. 6-8 thereof). However, in Miller, the "phase deference between the two signals arises from differences in signal path lengths and in the inherent delays" (column 8, lines 23-26 thereof), not arising from a different value held in a BSC. In addition, as shown in FIGS. 6-8 of Miller, both of the test and reference signals have a single pattern (P) periodically repeated "as is." That is, the "phase deference" in Miller is a delay (or shift) of a single phase pattern, and no signal in Miller has two phases. In addition, in Miller, the test signal is produced by a timing unit **46** in each channel (column 7, lines 59-61 thereof) and the reference signal is generated by a reference signal generator **58** (column 8, lines 3-5 thereof). Thus, in Miller, two different signals having the same phase pattern are compared, contrary to the claimed invention where a default phase and a sampled phase of the same AC signal is compared. In addition, Miller only correlates the two signals, and does not actually capture or sample the phase of the test signal, since the test signal has only one phase, as discussed above. Therefore, Miller

fails to teach or suggest capturing a default phase of said AC signal in response to said sync pulse signal, sampling a phase of the AC signal, and comparing the default phase with the sampled phase of the AC signal, as recited in claim 1.

Accordingly, Wu, whether considered alone or combined with or modified by Miller, does not teach or suggest, among others, generating an AC signal based on the reference clock and a value held in the BSC of the transmitting IC, the AC signal having a first phase if a first value is held in the BSC holds, and a second phase if a second value is held in the BSC, capturing, in the BSC of the receiving IC, a default phase of said AC signal in response to said sync pulse signal, sampling a phase of the AC signal, and comparing the default phase with the sampled phase of the AC signal, as recited in claim 1.

Claims 8 and 15 also include, among others, substantially the same distinctive features as claim 1. Therefore, it is respectfully requested that the rejection of claims based on Wu and Miller be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

2. Regarding claims 22-25

Claim 22 defines an output AC boundary scan cell (BSC). The claimed BSC comprises (a) a first flip-flop having a data input connected to a *bscanShiftIn* line, a clock input connected to a *clockBscanAc* line, a test reset input connected to a *testBscanAc* line, and an output connected to a *bscanShiftOut* line, (b) a second flip-flop having a data input

connected to said output of said first flip-flop, an update input connected to a *updateBscanAc* line, and a second flip-flop output, (c) an XOR logic gate having a first input connected to a *refClk* line, a second input connected to said second flip-flop output, and an XOR logic gate output, said XOR logic gate is adapted to output an AC signal, the AC signal having a first phase if a first value is held in said second flip-flop holds, the AC signal having a second phase if a second value is held in said second flip-flop, (d) and a multiplexer having a first input connected to a *fromCore* line, a select input connected to a *selectJtagOut* line, a second input connected to said XOR logic gate output, and a multiplexor output, said multiplexer selectively outputting a signal from the second input if a mode signal on the *selctJtagOut* line indicates an AC JTAG mode, as recited in claim 22 as amended.

Claim 23 defines an output AC boundary scan cell (BSC) for generating a signal. The claimed output AC BSC comprises (a) a first flip-flop for receiving and capturing a shift-in test data, (b) a second flip-flop connected to said first flip-flop for holding and updating a value of the shift-in test data, (c) an XOR logic gate connected to said second flip-flop for generating an AC signal based on a reference clock signal and the value held in said second flip-flop, the AC signal having a first phase if a first value is held in said second flip-flop, and having a second phase if a second value is held in said second flip-flop, and (d) a multiplexor for selectively outputting the AC signal based on a mode signal, as recited in claim 23 as amended.

Claim 24 defines an input AC boundary scan cell (BSC). The claimed input AC BSC comprises (a) a first flip-flop having a data input for receiving an input signal, a clock input connected to a *refClk* line, and a first flip-flop output, the input signal being an AC signal if said BSC is in an AC JTAG mode and a DC signal if said BSC is a non-AC JTAG mode, the first flip-flop output indicating a captured phase of the AC signal if the input signal is the AC signal, (b) a first multiplexer having a first input, a select input connected to a *syncPulse* line, a second input connected to said first flip-flop output, and a first multiplexer output, a sync pulse signal on the *syncPulse* line having an initial pulse, (c) a second flip-flop having a data input connected to said first multiplexer output, a clock input connected to a *refClk* line, and a second flip-flop output feedback to said first input of said first multiplexer, said second flip-flop adapted to capture a default phase of the AC signal in the AC-JTAG mode when the sync pulse signal has the initial pulse, the second flip-flop output indicating the default phase, (d) an XOR logic gate having a first input connected to said second flip-flop output, a second input connected to said first flip-flop output, and an XOR logic gate output, the XOR logic gate output having a first level if the first flip-flop output and the second flip-flop output match, and having a second level if the first flip-flop output and the second flip-flop output do not match, (e) a second multiplexer having a first input connected to said first flip-flop output, a select input connected to an *acjtagMode* line, a second input connected to said XOR logic gate output, and a second multiplexer output, (f) a third multiplexer having a first input connected to a *bscanShiftIn* line, a select input connected to a *ShiftBscan2Edge* line, a second input connected to said second multiplexer output, and a third multiplexer output, and (g) a third flip-flop having a first input connected to said third multiplexer

output, a second input connected to a *clockBscan* line, and a third flip-flop output connected to a *bscanShiftOut* line, as recited in claim 24 as amended.

Claim 25 defines an input AC coupled boundary scan cell (BSC) for receiving a signal. The claimed BSC comprises (a) a sampling flip-flop for sampling an input signal in accordance with a reference clock, the input signal being an AC signal if said BSC is in an AC JTAG mode, the sampling flip-flop adapted to capture and output a phase of the AC signal if the input signal is the AC signal, (b) a feedback flip-flop connected to said sampling flip-flop, said feedback flip-flop adapted to capture a default phase of the AC signal when a sync pulse signal has an initial pulse, an output of said feedback flip-flop indicating the default phase, and (c) an XOR logic r connected to the output of said sampling flip-flop and the output of said feedback flip-flop, an output of said XOR logic gate output having a first level if the output of said sampling flip-flop and the output of said feedback flip-flop match, and having a second level if the output of said sampling flip-flop and the output of said feedback flip-flop do not match, as recited in claim 25 as amended.

Therefore, the arguments regarding Wu and Miller set forth above are equally applicable to claims 22-25. It is respectfully requested that the rejection of claims based on Wu and Miller be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-3 depend from claim 1, claims 9-10 depend from claim 8, claims 16-17 depend from claim 15, claim 26 depends from claim 26, and thus include the limitations of respective independent claims. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-1698.

Respectfully submitted,
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Limited Recognition under 37 CFR §10.9(b)

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